Integrated Precision Battery Sensor for Automotive Systems

Silicon Anomaly

ADuC7036

This anomaly list describes the known bugs, anomalies, and workarounds for the ADuC7036 integrated precision battery sensor. The anomalies listed apply to all ADuC7036 packaged material branded as follows:

First Line ADuC7036
Second Line BCPZ, CCPZ, or DCPZ

Analog Devices, Inc., is committed, through future silicon revisions, to continuously improving silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems by implementing the recommended workarounds outlined here.

ADUC7036 FUNCTIONALITY ISSUES

Kernel Revision Identifier	Chip Marking	Silicon Status	Anomaly Sheet	No. of Reported Anomalies
A40 A60	ADuC7036 BCPZ or ADuC7036 CCPZ or ADuC7036 DCPZ	Release	Rev. C	3

ADUC7036 PERFORMANCE ISSUES

Kernel Revision Identifier	Chip Marking	Silicon Status	Anomaly Sheet	No. of Reported Anomalies
A40 A60	ADuC7036 BCPZ or ADuC7036 CCPZ or ADuC7036 DCPZ	Release	Rev. C	2

Rev. C

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FUNCTIONALITY ISSUES

1. Power-On Reset [er001]

Background	The ADuC7036 integrates a power-on reset (POR) circuit holding the ASIC in reset for 20 ms typically, after VDD reaches 3 V typically.
Issue	Under particular conditions, the POR does not release the reset signal, that is, the ASIC remains in reset until a power cycle occurs. This POR issue only occurs under three specific and coincident power-on conditions: • Fast ramp on VDD, nominally faster than 100 µs from V_{init} to 12 V. • Initial value of VDD (V_{init}) = ~1.2 V. • Voltage on REG_DVDD at the time VDD ramp is reapplied = ~175 mV.
Workaround	As previously noted, a fast VDD ramp (that is, ramping from ~1.2 V to 12 V in <100 µs) is required as one of the conditions required to initiate the reported POR issue. Analog Devices recommends careful selection of external power supply decoupling components to ensure that the VDD supply ramp rate can always be guaranteed to be >100 µs under all VBAT power-on conditions. Specifically, Analog Devices recommends a 10 Ω series resistor (1% tolerance maximum) and a 10 µF decoupling capacitor (20% tolerance maximum) to be connected to ground on the VDD line between the reverse protection diode and VDD, as shown in Figure 1.
Related Issues	None.

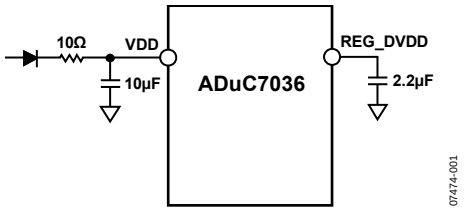

Figure 1.

2. LIN Short-Circuit Protection [er002]

Background	The ADuC7036 integrates a short-circuit protection feature.
Issue	Under particular conditions, a LIN short-circuit event can damage the ADuC7036. This damage only occurs under three specific and coincident conditions: • The ADuC7036 LIN pin is only connected to the LIN bus via a series inductor. • VBAT is greater than or equal to 18 V. • A LIN short circuit occurs while the LIN driver is driving the LIN bus low.
Workaround	Analog Devices recommends using a series resistor on the LIN pin to limit the amplitude voltage spike induced by the inductor when the short circuit to VBAT occurs. This voltage should not exceed the absolute maximum ratings of the LIN pin (40 V maximum). In the case of a 33 µH series inductor (10% tolerance), Analog Devices recommends using a 27.4 Ω series resistor (5% tolerance maximum), as shown in Figure 2.
Related Issues	None.

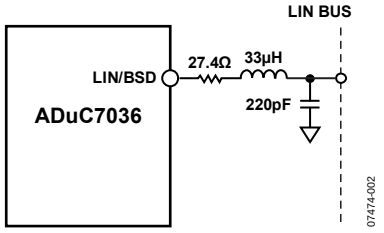

Figure 2.

3. ADC Overrange [er003]

Background	The ADuC7036 integrates a number of flags or status bits (ADCSTA[14:12]) to monitor overrange and underrange conditions in the ADC interface. These bits, automatically set by the hardware, are set to 1 to indicate an underrange or overrange has occurred in the ADC conversion. When this occurs, the data in the data register (ADCxDAT) is invalid. The conversion result in the data register (ADCxDAT) is clamped to negative full scale (underrange) or positive full scale (overrange).
Issue	Under certain limited operating conditions, a large negative overrange does not produce the expected clamp to negative full scale. Two situations may occur: • Issue 1: A clamp to positive full scale can occur with the error bits (ADCSTA[14:12] set correctly. • Issue 2: The error bits are not set correctly, and the ADC data register is not clamped to positive full scale or negative full scale. This occurs when the ADCFLT register has the following settings: ADCFLT[15] = 1 and ADCFLT[6:0] = 0x7E or 0x7F.
Workaround	A workaround for these two issues, when using the I-ADC, are as follows: • Issue 1: The error bits (ADCSTA[14:12] can be monitored to identify an overrange or underrange condition in the ADC conversion. • Issue 2: It is recommended not to use these two ADC filter configurations (ADCFLT[6:0] = 0x7E or 0x7F, when ADCFLT[15] = 1). If it is necessary to use these configurations, a workaround for the I-ADC is available by using the overrange (ADCSTA[3]) bit in the ADCSTA register. Two configurations are available. • This can be configured to produce an interrupt whenever the I-ADC input becomes grossly (133% of full scale) overrange in the positive or negative direction. Therefore, this interrupt, or status bit, can be monitored to indicate that the input has overranged, allowing the PGA gain to be changed without having to wait until the full ADC conversion is complete. • If an interrupt is not required, this bit can be used as an additional validation of the data register. The I-ADC data register (ADC0DAT) is valid if ADCSTA[0] is 1 and ADCSTA[3] is 0.

PERFORMANCE ISSUES

1. ESD [pr001]

Background	The ADuC7036 is intended to be classified for an HBM ESD rating of 2 kV.
Issue	The ADuC7036 HBM ESD is specified to 1 kV.
Workaround	Pending.
Related Issues	None.

2. WU Pin Latch-Up [pr002]

Background	The operating voltage of the WU pin is −3 V to +33 V.
Issue	There is a latch-up condition on the WU pin if a voltage below −1 V is applied on this pin.
Workaround	It is recommended to use a protection diode such as a BAS52, as shown in Figure 3, to avoid destructive damage to the part.
Related Issues	None.

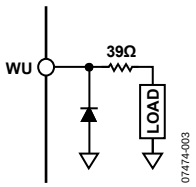

Figure 3. Protection Diode on WU Pin

SECTION 1. ADuC7036 FUNCTIONALITY ISSUES

Reference Number	Description	Status
er001	Power-on reset	Open
er002	LIN short-circuit protection	Open
er003	ADC overrange	Open

SECTION 2. ADuC7036 PERFORMANCE ISSUES

Reference Number	Description	Status
pr001	ESD	Open
pr002	WU pin latch-up	Open

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